

ABSTRACT

The present invention is directed to a multi-port memory device responsive to two systems. The device includes an array of memory cells each represented by a unique row and column address. The memory device has first and second input/output ports and an input/output control circuit, responsive to the first and second input/output ports, for writing data into and reading data of the array. The device further includes a first signal decoder responsive to the first system for producing first signals for accessing a cell within said array. The device also includes a second signal decoder responsive to the second system for producing second signals for accessing a cell within the array. A control circuit is responsive to the first and second systems for identifying which of the systems is entitled to access to the array in the event both systems seek access to the same address at the same time. The address and data associated with the address from the system not having access are saved so that the operation can be performed when access is granted.